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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/724,384	11/26/2003	Mark M. Leather	00100.01.0025	9662

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EXAMINER	
LAY, MICHELLE K	

ART UNIT	PAPER NUMBER
2628	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/724,384	LEATHER ET AL.	
	Examiner	Art Unit	
	MICHELLE K. LAY	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 September 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,6-9,12,14-17 and 22-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,6-9,12,14-17 and 22-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Please Note: Method claims 9, 12 and 14-16 are statutory under 35 USC 101 because the method is tied to an apparatus (i.e., front-end, back-end of graphics chip, geometry placed in frame buffer, parallel pipelines comprise unified shader).

Response to Amendment

The amendment filed 09/03/2008 has been entered and made of record. Claims 1, 4, 6-9, 12, 14-17, and 20-26 are pending. The amendment to the disclosure (09/03/2008) has overcome the 35 USC 101 rejection made in the non-final office action (06/03/2008).

Response to Arguments

Applicant's arguments, filed 09/03/2008, have been fully considered and are persuasive. The non-final rejection filed 06/03/2008 has been withdrawn.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims **1**, **4**, **7-9**, **12**, **14-17**, **20**, and **22-26** are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhu (6,697,063 B1) in view of Rosman et al. (6,222,550 B1) and Sperber et al. (6,557,083).

Zhu teaches the limitations of claims 1, 4, 7-9, 12, 14-17, 20, and 22-26 with the exception of explicitly teaching multiple parallel pipelines and a single graphics chip. However, Rosman teaches a 3D graphics processor with parallel triangle pixel pipelines [abstract] and Sperber teaches an integrated-circuit die in which a processor core and graphics core are integrated on a single chip [c.4 L.25-30].

In regards to claim **1**, Zhu teaches a rendering pipeline system using screen space tiling that uses double-z scheme that decouples scan conversion/depth-buffer processing from the more general rasterization and shading processing through a scan/z engine [abstract]. With reference to Fig. 4, the geometries in model space (401) are transformed into screen space and the screen space tiler (412) bins a frame worth of geometries into screen tiles (said ***defined by tiles***). The visibility of all geometries is determined up front using screen x, y, z coordinates (402) are determined in the scan/z engine (403) [c.5 L.45-50]. Thus, the screen space tiler (412) and tile scan/z engine (403) comprises said ***front-end***, where the output (404) of the tile scan/z engine (403) is sent to raster engine (405), shading engine (said ***unified shader***) (406), and blending engine (407) [c.5 L.51-60]. The raster engine (405), shading engine (406), and blending engine (407) comprise said ***back-end***.

Rosman teaches a 3D graphics processor having parallel pipelines (said ***multiple parallel pipelines***). A hardware accelerated Geometry Engine (said ***front-end***) may supply the vertices of triangles to triangle setup engine (28) [c.6 L.25-32]. The triangle setup engine (28) [Fig. 3] directs the gradients and vertices to the triangle pixel-pipelines (40, 41) [c.6 L.33-35]. Once a triangle is setup by triangle setup engine (28), its gradients and vertices are sent to the next available triangle pixel-pipeline(s) (40, 41) (said ***back-end***). Triangle pixel-pipelines (40, 41) are each pixel engines (PE) that receive the three vertices for a triangle. Triangle pixel pipelines (40, 41) output pixel values to a frame buffer [c.6 L.33-45].

It would have been obvious to one of ordinary skill in the art to modify the system of Zhu with the parallel pipelines of Rosman because implementing parallel processing results in multiplying the pixel throughput [Rosman: c.2 L.15-17].

Sperber teaches an integrated-circuit die in which a processor core (310) and graphics core (320) are integrated on a single chip [Fig. 3; c.4 L.20-35].

Therefore, it would have been obvious to one of ordinary skill is the art to implement the modified front-end of Zhu in view of Rosman into the processor core of Sperber, and the back-end of Zhu in view of Rosman into the graphics core of Sperber because it is known in the art that significant amount of rendering causes a burden on the bandwidth of the memory channel, which in turn can reduce the performance of the graphics system. Furthermore, memory demands by the graphic engine can reduce CPU performance, as well as other units [Sperber: c.2 L.13-31]. Thus, by implementing both the front-end and back-end of Rosman on a single chip, the interfaces between

units are reduced in size, resulting in a faster interaction. Additionally, the single chip occupies less real estate within the system, therefore providing either a smaller system overall, or more space for other internal devices.

In regards to claim **4**, Zhu teaches using ***FIFO*** buffers between the scan/z engine (said front-end) and raster/shading/blending engine (said back-end) to load balance the computations [c.13 L.4-7].

In regards to claim **6**, Zhu teaches double-z method that decouples pixel shading rate from scan conversion and z-buffer rate. The system includes a tile scan/z with depth buffer (403) (said ***z-buffer***) and color frame buffer (409) (said ***color buffer***) [c.9 L.46-67; Fig. 4]. In both cases, logic is needed to implement the process of both buffers.

In regards to claim **7**, Zhu teaches double-z method that decouples pixel shading rate from scan conversion and z-buffer rate [c.5, L.29-31]. Thus the interface from the memory to the tile scan/z engine (403) functions as said ***early Z interface*** where Memory functions as the ***hierarchical z interface***.

In regards to claim **8**, Zhu teaches double-z method that decouples pixel shading rate from scan conversion and z-buffer rate [c.5, L.29-31]. Thus the interface from the texture memory to the shading engine (406) functions as said ***late Z interface*** where Memory functions as the ***hierarchical z interface***.

In regards to claim **25**, Zhu teaches screen space tiling (SST) partitions a screen into disjoint regions called tiles (said ***geometry defined by a tile***) [c.6 L.3-4] where the geometry (404) is then sent to the raster (405) [Fig. 4]. In the modified system of Zhu in view of Rosman, Rosman teaches a hardware accelerated Geometry Engine may supply the vertices of triangles to triangle setup engine (28) [c.6 L.25-32]. The triangle setup engine (28) (said ***setup unit***) [Fig. 3] directs the gradients and vertices to the triangle pixel-pipelines (40, 41) (said ***directing said geometry into pipelines***) [c.6 L.33-35]. Once a triangle is setup by triangle setup engine (28), its gradients and vertices are sent to the next available triangle pixel-pipeline(s) (40, 41) [c.6 L.33-45]. Therefore, by implementing the pipeline of Zhu in multiple parallel fashion as taught by Rosman, the triangle set up engine (28) would be needed in the modified system of Zhu in order to direct the different geometries to the multiple pipelines. The same rationale for combining as applied to claim 1 is incorporated herein.

In regards to claim **26**, with reference to Fig. 4 of Zhu, the pipeline comprises tile scan/z engine (403) (said ***scan converter***), raster engine (405) (said ***rasterizer***), and shading engine (406) (said ***texture unit***) [c.5 L.46-60].

In regards to claim **9**, claim 9 recites similar limitations as claim 1 but in process form. Therefore, the same rationale used for claim 1 is applied. Furthermore, it would have been obvious to one of ordinary skill in the art that the modified system of Rosman implements a process.

In regards to claim **12**, claim 12 recites similar limitations as claim 4 but in process form. Therefore, the same rationale used for claim 4 is applied. Please refer to claim 9 for the rationale of process means.

In regards to claim **14**, claim 14 recites similar limitations as claim 6 but in process form. Therefore, the same rationale used for claim 6 is applied. Please refer to claim 9 for the rationale of process means.

In regards to claim **15**, claim 15 recites similar limitations as claim 7 but in process form. Therefore, the same rationale used for claim 7 is applied. Please refer to claim 9 for the rationale of process means.

In regards to claim **16**, claim 16 recites similar limitations as claim 8 but in process form. Therefore, the same rationale used for claim 8 is applied. Please refer to claim 9 for the rationale of process means.

In regards to claim **17**, claim 17 recites similar limitations as claim 1 but in manufacture form. Therefore, the same rationale used for claim 1 is applied. Furthermore, it would have been obvious to one of ordinary skill in the art that instructions are sent to the system of Rosman in order to implement the process.

In regards to claim **20**, claim 20 recites similar limitations as claim 4 but in manufacture form. Therefore, the same rationale used for claim 4 is applied. Please refer to claim 17 for the rationale of manufacture means.

In regards to claim **22**, claim 22 recites similar limitations as claim 6 but in manufacture form. Therefore, the same rationale used for claim 6 is applied. Please refer to claim 17 for the rationale of manufacture means.

In regards to claim **23**, claim 23 recites similar limitations as claim 7 but in manufacture form. Therefore, the same rationale used for claim 7 is applied. Please refer to claim 17 for the rationale of manufacture means.

In regards to claim **24**, claim 24 recites similar limitations as claim 8 but in manufacture form. Therefore, the same rationale used for claim 8 is applied. Please refer to claim 17 for the rationale of manufacture means.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. .

Perego (6,864,896 B2)

Deering (4,885,703)

Regan (6,407,736 B1)

Donham et al. (6,980,209 B1)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michelle K. Lay whose telephone number is (571) 272-7661. The examiner can normally be reached on Monday-Friday 7:30a-5p.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee M. Tung can be reached on (571) 272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Michelle K. Lay/
Examiner, Art Unit 2628
5 December 2008